IN THE SPECIFICATION:

Please replace paragraph number **[0052]** of the specification with the following:

[0052] FIGs. 12-16 illustrate yet another embodiment of a semiconductor device structure 40 that incorporates teachings of the present invention. With reference to FIGs. 12 and 13, semiconductor device structure 40 includes dual damascene trenches 44 formed in a surface 42 of an insulator layer 41 thereof. As shown, one or more of trenches 44 may expose a conductively doped region 23 of a semiconductor substrate 21 of semiconductor device structure 40, which conductively doped region 23 is continuous with a surface 22 of semiconductor substrate 21. A conductive layer 46 overlies surface 42 and substantially fills trenches 44. Conductive layer 46 has a nonplanar upper surface 47 that includes valleys 54 located substantially over trenches 44 and peaks 52 located substantially over surface 42. Insulator layer 41, trenches 44, and conductive layer 46, as well as other structures of semiconductor device structure 40 underlying insulator layer 41 and trenches 44 are each fabricated by known processes, such as those disclosed in U.S. Patent 5,980,657 to Farrar et al. on November 9, 1999, the disclosure of which is hereby incorporated in its entirety by this reference.

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